IN THE CLAIMS:

Please amend claims 3 and 15, as shown in the complete list of claims that is presented below.

Claims 1 and 2 (cancelled).

3. (currently amended) A dry etching method for a semiconductor device, comprising:

providing a polysilicon layer formed on a silicon substrate;

implanting a first region of the polysilicon layer with N type ions and a second region of the polysilicon layer with P type ions, a further region of the polysilicon layer being left as a non-doped region;

simultaneously gate-etching an N type polysilicon gate electrode from the first region, a P type polysilicon gate electrode from the second region, and a non-doped polysilicon dummy gate arrangement from the non-doped region of the polysilicon layer during a two-stage etching process;

wherein the N type polysilicon gate electrode has an area that is smaller than the area of the first region of the polysilicon layer and the P type polysilicon gate electrode has an area that is smaller than the area of the second region of the polysilicon layer,

wherein the etched area of the non-doped polysilicon ~~dummy gate arrangement has an area that~~ region is larger than the ~~total~~ sum of the etched area of the first region of the ~~occupied by the N type~~ polysilicon ~~gate electrode~~ layer and the etched area of the second region of the ~~P type~~ polysilicon ~~gate electrode~~ layer, and

wherein an end point detection of one of the stages of the etching process is based on the etching of the non-doped polysilicon dummy gate arrangement.

Claim 4 (cancelled).

5. (previously presented) The dry etching method according to claim 3, wherein the two-stage etching includes a first stage using a mixed gas of HBr and O_2 and a second stage using a mixed gas of HBr, O_2 and He.

Claims 6-10 (cancelled).

11. (previously presented) The dry etching method according to claim 3, wherein the N type polysilicon gate electrode and the P type polysilicon gate electrode are disposed adjacent one another.

Claims 12-13 (cancelled).

14. (previously presented) The dry etching method of claim 3, wherein the non-doped polysilicon dummy gate arrangement is disposed adjacent to at least one of the N type polysilicon gate electrode and the P type polysilicon gate electrode.

15. (currently amended) A dry etching method for a semiconductor device, comprising:

providing a polysilicon layer formed on a semiconductor substrate;

implanting a first region of the polysilicon layer with N type ions and a second region of the polysilicon layer with P type ions, a further region of the polysilicon layer being left as a non-doped region; and

simultaneously etching an N type polysilicon gate electrode from the first region, a P type polysilicon gate electrode from the second region, and a non-doped polysilicon dummy gate arrangement from the non-doped region of the polysilicon layer during a multi-stage etching process,

wherein the N type polysilicon gate electrode has an area that is smaller than the area of the first region of the polysilicon layer and the P type polysilicon gate electrode has an area that is smaller than the area of the second region of the polysilicon layer,

wherein the etched area of the non-doped polysilicon ~~dummy gate arrangement has an area that~~ region is larger than the ~~total~~ sum of the etched area of the first region of the ~~occupied by the N type~~ polysilicon ~~gate electrode~~ layer and the etched area of the second region of the ~~P type~~ polysilicon ~~gate electrode~~ layer, and

wherein the etching process includes at least one etching stage in which end point detection is based on the etching of the non-doped polysilicon dummy gate arrangement.

16. (previously presented) The dry etching method according to claim 15, wherein the non-doped polysilicon dummy gate arrangement is disposed adjacent at least one of the P type polysilicon gate electrode and the N type polysilicon gate electrode.

17. (previously presented) The dry etching method according to claim 15, wherein the P type polysilicon gate electrode is disposed adjacent to the N type polysilicon gate electrode.

18. (previously presented) The dry etching method according to claim 15, wherein the at least one etching stage is conducted using a mixed gas of HBr and O_2.

19. (previously presented) The dry etching method according to claim 15, wherein the at least one etching stage is conducted using a mixed gas of HBr, O_2, and He.

Claims 20-21 (cancelled).